AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A display unit comprising:

a display panel comprising a pixel matrix comprising:

a rectangular pixel frame buffer region; and

a fixed, active pixel border region comprising pixels permanently dedicated to displaying a border attribute, wherein said fixed, active pixel border region surrounds said rectangular pixel frame buffer region on four sides of said rectangular pixel frame buffer region and comprises a width in the range of two to ~~of less than~~ 128 pixels;

a frame buffer memory for containing image data for generating an image within said frame buffer region;

a border attribute register dedicated for containing said border attribute, wherein said border attribute is automatically selected to provide viewing contrast with image data located near said border region, and wherein said border attribute comprises color information for each pixel in said fixed, active pixel border region, and wherein said border attribute is equal to a background attribute currently being displayed; and

a display controller coupled to said frame buffer memory, coupled to receive said border attribute from said border attribute register, and coupled to control said display panel, said display controller for generating a first set of signals for rendering said image within said frame buffer region and for generating a second set of signals for displaying said border attribute within said fixed, active pixel region.

2. (Currently Amended) The [[A]] display unit as described in Claim 1 wherein said second set of signals are generated within invalid timing windows with respect to said frame buffer region.

3. (Currently Amended) The [[A]] display unit as described in Claim 1 wherein a first portion of said second set of signals are generated in an invalid horizontal timing window that commences x clock cycles before valid data for said frame buffer region commences and wherein a second portion of said second set of signals are generated in an invalid horizontal timing window that ends x clock cycles after valid data for said frame buffer region completes.

4. (Currently Amended) The [[A]] display unit as described in Claim 3 wherein a third portion of said second set of signals are generated in an invalid vertical timing window that commences x horizontal pulses before a first valid horizontal line commences of a frame and wherein a fourth portion of said second set of signals are generated in an invalid vertical timing window that ends x horizontal pulses after the end of the last valid horizontal line of said frame.

5. (Currently Amended) The [[A]] display unit as described in Claim 1, wherein said border attribute of said border region comprises a color attribute.

6. (Currently Amended) The [[A]] display unit as described in Claim 1 wherein said display panel is a thin film transistor liquid crystal display panel.

7. (Canceled).

8. (Currently Amended) The [[A]] display unit as described in Claim 1 wherein said frame buffer region comprises 160 rows and 160 columns of pixels.

9. (Currently Amended) The [[A]] display unit as described in Claim 1 further comprising a background display attribute register and wherein, by default, said border attribute register is equal to said background attribute register.

10. (Currently Amended) A display unit comprising:

a display panel comprising a pixel matrix comprising: a rectangular pixel frame buffer region; and a fixed, active pixel border region comprising pixels permanently dedicated to displaying a border attribute, wherein said fixed, active pixel border region surrounds said rectangular pixel frame buffer region on four sides of said rectangular pixel frame buffer region including ~~and contains~~ top, bottom, right and left border regions, wherein said fixed, active pixel border region comprises a width in the range of two to ~~of less than~~ ten pixels;

a frame buffer memory for containing character data for generating character images within said frame buffer region;

a border attribute register dedicated for containing said border attribute for said border region, wherein said border attribute is automatically selected to provide viewing contrast with character images located near said border region, and wherein said border attribute comprises color information for each pixel in said fixed, active pixel border region, and wherein said border attribute is equal to a background attribute; and

a display controller coupled to said frame buffer memory, coupled to receive said border attribute of said border attribute register, and coupled to control said display panel, said display controller for generating a first set of

signals for rendering said character images within said rectangular pixel frame buffer region wherein said first set of signals comprises vertical and horizontal invalid timing windows and wherein said display controller is also for generating a second set of signals for displaying said border attribute within said fixed, active pixel region.

11. (Currently Amended) The [[A]] display unit as described in Claim 10 wherein said second set of signals are generated within said vertical and horizontal invalid timing windows.

12. (Currently Amended) The [[A]] display unit as described in Claim 10 wherein said top and bottom border regions are rendered during said vertical invalid timing windows and wherein said right and left border regions are rendered during said horizontal invalid timing windows.

13. (Currently Amended) The [[A]] display unit as described in Claim 10 wherein said display attribute comprises a color attribute.

14. (Currently Amended) The [[A]] display unit as described in Claim 10 wherein said display panel is a thin film transistor liquid crystal display panel.

15. (Canceled).

16. (Currently Amended) The [[A]] display unit as described in Claim 10 wherein said frame buffer region comprises 160 rows and 160 columns of pixels.

17. (Currently Amended) The [[A]] display unit as described in Claim 10 further comprising a background display attribute register and wherein, by default, said border attribute register is equal to said background attribute register.

18. (Currently Amended) A handheld device comprising:

a processor;

a memory unit coupled to said processor; and

a display unit coupled to said processor and comprising:

a display panel comprising a pixel matrix comprising: a rectangular pixel frame buffer region; and a fixed, active pixel border region comprising pixels permanently dedicated to displaying a border attribute, wherein said fixed, active pixel border region surrounds said rectangular pixel frame buffer region on four sides of said rectangular pixel frame buffer region and comprises a width in the range of two to ~~of less than~~ five pixels;

a frame buffer memory for containing image data for generating an image within said rectangular pixel frame buffer region;

a border attribute register dedicated for containing said border attribute for said fixed, active border region, wherein said border attribute is automatically selected to provide viewing contrast with image data located near said fixed, active border region, and wherein said border attribute comprises color information, and wherein said border attribute is equal to a background attribute currently being displayed; and

a display controller coupled to said frame buffer memory, coupled to receive said border attribute from said border attribute register, and

coupled to control said display panel, said display controller for generating a first set of signals for rendering said image within said rectangular pixel frame buffer region and for generating a second set of signals for displaying said border attribute within said fixed, active pixel region.

19. (Currently Amended) The [[A]] handheld device as described in Claim 18 wherein said second set of signals are generated within video timing windows that contain invalid data with respect to said frame buffer region.

20. (Currently Amended) The [[A]] handheld device as described in Claim 18 wherein a first portion of said second set of signals are generated x clock cycles before valid data for said frame buffer region commences and wherein a second portion of said second set of signals are generated x clock cycles after valid data for said frame buffer region completes.

21. (Currently Amended) The [[A]] handheld device as described in Claim 18 wherein said display attribute comprises a color attribute.

22. (Currently Amended) The [[A]] handheld device as described in Claim 18 wherein said display panel is a thin film transistor liquid crystal display panel.

23. (Currently Amended) The [[A]] handheld device as described in Claim 18 further comprising a background display attribute register and wherein, by default, said border attribute register is equal to said background attribute register.